

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	3,691,534	09/12/72	Veradi, et. al	365	78	
	3,771,145	11/06/73	Wiener	365	240	
	4,231,104	10/28/80	St.Clair	713	500	
	4,466,127	08/14/84	Ohgishi, et. al	455	182.1	
	4,536,795	08/20/85	Hirota, et. al	348	714	
	4,616,268	10/07/86	Shida, et. al	358	451	
	4,629,909	12/16/86	Cameron	327	211	
	4,631,659	12/23/86	Hayne, et. al	711	167	
TNT	4,648,102	03/03/87	Riso, et. al	375	356	

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
TNT	EP 0424774	05/02/91	EPO			
TNT	EP 0449052	03/29/90	EPO			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	Takasugi, A. et al., "A Data-Transfer Architecture for Fast Multi-Bit Serial Access Mode DRAM," 11 th European Solid State Circuits Conference, Toulouse, France pp.161-165 (Sep. 1985)
TNT	Amitai, Z., "Burst Mode Memories Improve Cache Design," WESCON/90 Conference Record, pp.29-32 (Nov. 1990)
TNT	Ikeda, Hiroaki et al., "100 MHz Serial Access Architecture for 4Md Field Memory," Symposium of VLSI Circuits, Digest of Technical Papers, pp. 11-12 (Jun. 1990)
TNT	Schmitt-Landsiedel, Doris, "Pipeline Architecture for Fast CMOS Buffer RAMs," IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, pp. 741-747 (Jun. 1990)

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TNT	4,663,735	05/05/87	Novak, et. al	345	515	
	4,672,470	06/09/87	Morimoto, et. al	386	16	
	4,719,505	01/12/88	Katznelson	348	502	
	4,825,287	04/25/89	Baji, et. al	348	720	
	4,845,677	07/04/89	Chappell, et. al	365	189.02	
	4,873,671	10/10/89	Kowshik, et. al	365	189.12	
	4,876,670	10/24/89	Nakabayashi, et. al	365	194	
TNT	4,901,036	02/13/90	Herold, et. al	331	25	

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
TNT	EP 0218523	05/30/89	EPO			
TNT	EP 0282735	09/21/88	EPO			

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TNT	K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986)
TNT	Horowitz et al., "MIPS-X: A 20-MIPS Peak 32-Bit Microprocessor with ON-Chip Cache", IEEE J. Solid State Circuits, vol. SC-22, No. 5, pp. 790-798 (Oct. 1987)
TNT	Robert J. Lodi et al., "Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit," 1976 IEEE International Solid-State Circuits Conference (Feb. 18, 1976)

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TNT	4,979,145	12/18/90	Remington, et. al	711	106	
	5,009,481	04/23/91	Kinoshita, et. al	385	33	
	5,016,226	05/14/91	Hiwada, et. al	365	233	
	5,036,495	07/30/91	Busch, et. al	365	233	
	5,111,486	05/05/92	Oliboni, et. al	375	120	
	5,123,100	06/16/92	Hisada, et. al	713	401	
	5,142,376	08/25/92	Ogura	386	29	
TNT	5,276,846	01/04/94	Aichelmann Jr., et. al	711	165	

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TNT	Whiteside, Frank, "A Dual-Port 65ns 64Kx4 DRAM with a 50MHz Serial Output," IEEE International Solid-State Circuits Conference Digest (Feb. 1986)

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TNT	5,301,278	04/05/94	Bowater, et. al	711	5	
1	5,361,277	11/01/94	Grover	375	38	
TNT	5,684,753	11/04/97	Hashimoto, et al	365	233	

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TNT	WO 89/12936	12/28/89	PCT			
	JP 62-51509	03/06/87	Japan			YES

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TNT	Pinkham, Raymond, "A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 6, pp. 999-1007 (Dec. 1984)
TNT	Ishimoto, S. et al., "A 256K Dual Port Memory," ISSCC Digest of Technical Papers, p. 38-39 (Feb. 1985)
TNT	Iqbal, Mohammad Shakaib, "Internally Timed RAMs Build Fast Writable Control Stores," Electronic Design, pp. 93-96 (August 25, 1988)
TNT	Schnaitter, William M. et al., "A 0.5-GHz CMOS Digital RF Memory Chip," IEEE Journal of Solid-State Circuits, vol. SC-21, no. 5, pp. 720-726 (Oct. 1986)
TNT	Bursky, Dave, "Advanced Self-Timed SRAM Pares Access Time to 5 ns," Electronic Design, pp. 145-147 (Feb. 22, 1990)
TNT	Tomoji Takada et al., "A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Memories," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989)

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TNT	Robert J. Lodi et al., "MNOS-BORAM Memory Characteristics," IEEE Journal of Solid-State Circuits, vol. SC-11, No. 5, pp. 622-631 (Oct. 1976)
TNT	Gregory Uvieghara et al., "An On-Chip Smart Memory for a Data-Flow CPU," IEEE Journal of Solid-State Circuits, vol. 25, No. 1, pp. 84-89 (Feb. 1990)
TNT	Ray Pinkham et al., "A 128Kx8 70-MHz Multiport Video RAM with Auto Register Reload and 8x4 WRITE Feature," IEEE Journal of Solid State Circuits, vol. 23, no. 3, pp. 1133-1139 (Oct. 1988)
TNT	Hans-Jurgen Mattausch et al., "A Memory-Based High-Speed Digital Delay Line with a Large Adjustable Length," IEEE Journal of Solid-State Circuits, vol. 23, no. 1, pp. 105-110 (Feb. 1988)
TNT	Kanopoulos, Nick and Jill H. Hallenbeck, "A First-In, First-Out Memory for Signal Processing Applications," IEEE Transactions on Circuits and Systems, Vol. CAS-33, No. 5, pp. 556-558 (May 1986)

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